

PATENT

App. Ser. No.: 10/039,017
Atty. Dkt. No. ROC920010189US1
PS Ref. No.: IBMK10189

IN THE CLAIMS:

Please cancel claims 8, 15 and 18-33 without prejudice, and amend the claims as follows:

1. (Currently Amended) A pipelined circuit apparatus for performing operations on a first binary number and a second binary number, comprising:
 - a first arithmetic logic unit (ALU) operating on a first lower portion of the first binary number and a second lower portion of the second binary number to produce a first result and a carry out signal; and
 - a second ALU operating on a first upper portion of the first binary number and a second upper portion of the second binary number to produce a second result; and
 - a logic circuit selecting one of the first upper portion and the second upper portion in response to the first flag bit and the second flag bit, the selected upper portion used as the second result;
 - wherein at least one stage in the pipelined circuit stalls by one or more clock cycles in response to the carry out signal to account for additional delay introduced by incrementing the second result when the carry out signal indicates a carry;
 - wherein the first binary number is associated with a first flag bit, the first flag bit indicating a first predetermined number of most significant bits of the first binary number are all zero; and
 - wherein the second binary number is associated with a second flag bit, the second flag bit indicating a second predetermined number of most significant bits of the second binary number are all zero.
2. (Original) The apparatus of claim 1 further comprising:
 - a memory having a first memory portion receiving the first result and a second memory portion receiving the second result.
3. (Previously Presented) The apparatus of claim 2 further comprising:

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a logic circuit for incrementing a value stored in the second memory portion when the carry out signal indicates a carry.

4. (Original) The apparatus of claim 3 wherein:
the incremented value is stored into the second memory portion in response to the carry out signal.
5. (Original) The apparatus of claim 2 wherein:
the second memory portion is configured to increment a value stored in the second memory portion in response to the carry out signal.
6. (Original) The apparatus of claim 2 wherein:
the memory stores a value used to address a random access memory.
7. (Original) The apparatus of claim 1 wherein:
the first binary number is split in two at a first bit boundary to form the first upper portion and the first lower portion; and
the second binary number is split in two at a second bit boundary to form the second upper portion and the second lower portion.
8. (Canceled) The apparatus of claim 1 wherein:
the first binary number is associated with a first flag bit, the first flag bit indicating a first predetermined number of most significant bits of the first binary number are all zero;
the second binary number is associated with a second flag bit, the second flag bit indicating a second predetermined number of most significant bits of the second binary number are all zero; and
the apparatus further comprising:

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a logic circuit selecting one of the first upper portion and the second upper portion in response to the first flag bit and the second flag bit, the selected upper portion used as the second result.

9. (Currently Amended) The apparatus of ~~claim 8~~ claim 1, further comprising:
at least two buffers for each bit position in the second result, each the buffer receiving a corresponding bit value within the second result, each the buffer driving an electrically conductive line that has minimum width.

10. (Original) The apparatus of claim 1 wherein:
the second binary number is split in two at a second bit boundary to form the second upper portion and the second lower portion.

11. (Currently Amended) A pipelined circuit apparatus, comprising:
an arithmetic logic unit (ALU) operating on two binary numbers, the ALU comprising:

a first logic circuit generating a carry out signal from a bit location that is not the most significant bit of the ALU;

wherein at least one stage of the pipelined circuit stalls by one or more clock cycles in response to the carry out signal to account for additional delay introduced by incrementing the second result when the carry out signal indicates a carry; and

a logic circuit selecting an upper portion of one of the two binary numbers, the selecting done in response to the first flag bit and the second flag bit;

wherein a first flag bit is associated with a first of the two binary numbers, the first flag bit indicating a predetermined number of most significant bits of the first binary number are all zero; and

wherein a second flag bit is associated with a second of the two binary numbers, the second flag bit indicating a predetermined number of most significant bits of the second binary number are all zero.

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12. (Original) The apparatus of claim 11, the ALU further comprising:
a first logic unit operating on lower portions of the two binary numbers to produce a first result;
a second logic unit operating on upper portions of the two binary numbers to produce a second result;
a second logic circuit for incrementing the second result in response to the carry out signal to form an incremented value.
13. (Original) The apparatus of claim 12 wherein:
a final result for the ALU is formed by combining:
the first result, and
selection of one of the second result and the incremented value, the selection being done in response to the carry out signal.
14. (Original) The apparatus of claim 12, the ALU further comprising:
a first memory storing the first result; and
a second memory conditionally storing either the second result or the incremented value, the condition determined in response to the carry out signal.
- 15.-33. (Canceled)